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A silicon-molecular hybrid memory device

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Abstract
We have fabricated MOS memory devices based on coil–rod–coil triblock molecules acting as quantum dots. Uniform molecular dots result in a discrete shift in the threshold voltage at room temperature, which is indicative of single-electron effects. Molecular scalability and low-power operation make the silicon-molecular hybrid device an attractive candidate for next-generation electronic devices.

1. Introduction

It is expected that future memory devices will be scaled down to the nanometre range. Nanometre scale devices utilizing the Coulomb blockade effect are promising candidates for becoming the basic elements of future electronics. However, fabrication of such devices demands cutting-edge nanolithography techniques. One way to implement a nanometre range structure without the lithography technique is to use nanomaterials such as nanocrystals, molecules, etc.

Recently, metal–oxide–semiconductor (MOS) structures using nanocrystals have been reported to show good memory effects [1–3]. In these nanocrystal nonvolatile memory devices, charge is stored in a discontinuous floating-gate layer composed of discrete crystalline nanocrystals. However, Coulomb blockade effects have been shown only below about 77 K due to the random size distribution of the nanocrystals [2]. For practical application, however, room temperature operation capability is required, which is made possible by small and uniform dots. In this paper, we describe the fabrication and electrical characterization of the memory devices based on the molecular dots, which show single-electron effects at room temperature.

2. Experimental procedure

The molecules used in our experiments are the coil–rod–coil triblock molecules consisting of three biphenyls connected through vinylene linkages as a conjugated rod segment and poly (prophylene oxide) as the coil segment. As shown in figure 1(a), these molecules prepared as described in [4] self-assemble into puck-like cylindrical-shaped-supramolecular rod-bundles. Each aggregate contains 83 rod segments and its dimension is 5 nm in diameter and 3 nm in length. The solid-state absorption spectra of these supramolecular rod-bundles exhibit an intense transition with a maximum of 350 nm, suggesting that the conjugated rod block acts as a quantum dot [5].

Figure 1(b) shows a schematic cross section of the fabricated device. It has a similar structure to the nanocrystal memory except that the supramolecular aggregates are placed in between the channel and the control gate instead of nanocrystals. The devices were fabricated on silicon-on-insulator (SOI) material formed using the separation by ion implantation of oxygen (SIMOX) process. The SOI wafer has a 150 nm-thick top silicon layer, separated from the underlying silicon substrate by a 80 nm-thick buried SiO_2 layer. A narrow channel of 100 nm in width and 600 nm in length was defined by electron-beam lithography and etched into the top silicon layer using reactive ion etching (RIE). Device fabrication continues by growing a 20 nm-thick control oxide at 1000 °C prior to the ohmic contact formation by evaporating aluminium and heating at 420 °C for 30 s. On this structure, the supramolecular aggregates were spread by dropping a supramolecular solution dissolved in hexane and drying the solvent. Finally, a 150 nm-thick SiO_2 was deposited by using plasma enhanced chemical vapour deposition (PECVD) and then the aluminium gate was formed.

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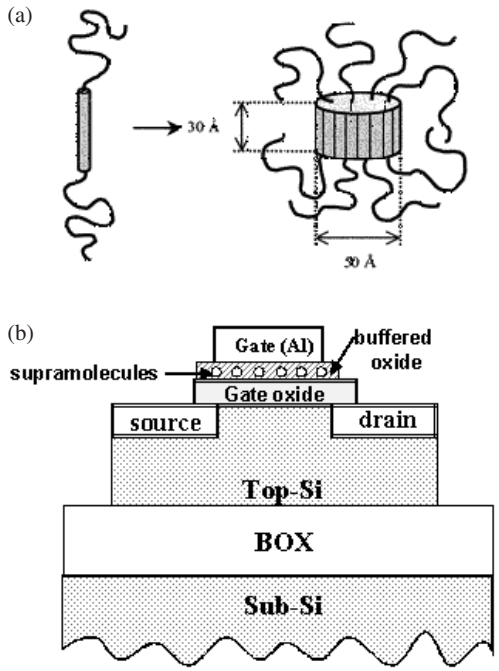

Figure 1. (a) Schematic representation of the self-assembly of coil–rod–coil molecules into a supramolecular bundle. (b) Schematic cross section of the fabricated memory device based on the supramolecular rod-bundles.

3. Results and discussion

Figure 2 shows the source/drain current–gate voltage characteristics (I_{SD}–V_G) measured at room temperature with the source/drain voltage V_{SD} of 0.1 V. Large hysteresis is observed implying the possibility of application in memory devices. However, in contrast to the device with nanocrystals showing the clockwise hysteresis [1–3], the counterclockwise hysteresis is observed and the negative threshold voltage shift ($\Delta V_T \approx -1$ V) is found. This result suggests that the application of V_G causes the electrons to tunnel from the molecules into the channel, since injection of electrons in the channel region results in a lower threshold voltage. Similar behaviours have been also observed by Li *et al* [6] on ferrocene-containing self-assembled monolayers. V_T is defined as the gate voltage corresponding to $I_{SD} = 10^{-10}$ A when $V_{SD} = 0.1$ V is applied. For comparison, the devices without the molecules were also fabricated. They have shown no hysteresis, indicating that the hysteresis is not caused by interface traps or mobile ions but by the depleted electrons in the supramolecular aggregates.

In order to observe the memory effect, a voltage pulse V_{GP} was applied to the gate and then the I_{SD}–V_G characteristics were measured with $V_{SD} = 0.1$ V. Figures 3(a) and (b) present the data obtained from the devices with the molecules and without the molecules, respectively. The device without the molecules exhibits the typical I_{SD}–V_G characteristics of a MOSET without any threshold voltage shift, whereas the device with the molecules shows two interesting features in figure 3(a). The first one is that the V_T is more shifted as V_{GP} increases. In figure 3(c), V_T is plotted as a function of V_{GP}. Staircase plateaus are shown with a discrete threshold voltage shift of about 0.5 V and each shift corresponds to a voltage

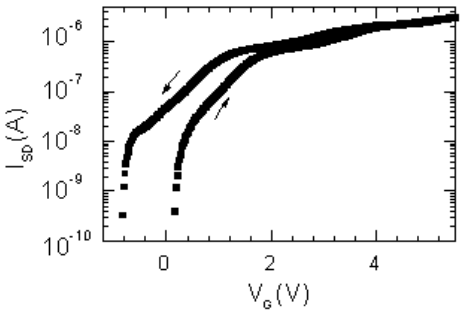

Figure 2. The I_{SD}–V_G characteristics measured with $V_{SD} = 0.1$ V by sweeping V_G forth and back.

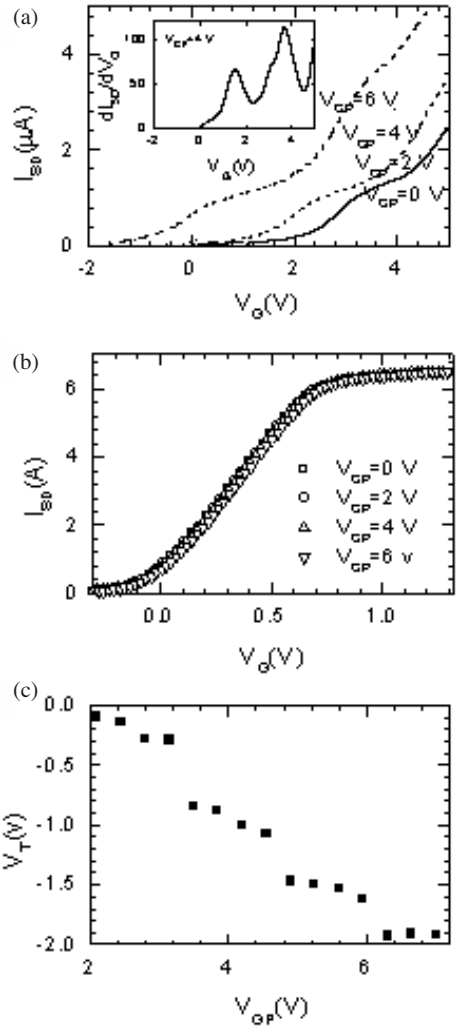

Figure 3. The I_{SD}–V_G characteristics measured with $V_{SD} = 0.1$ V after applying various voltage pulses to the gate for the memory devices with the molecules (a) and without the molecules (b). The inset shows dI_{SD}/dV_G as a function of V_G, where dI_{SD}/dV_G has been numerically calculated from the I_{SD}–V_G curve. (c) Threshold voltage V_T as a function of V_{GP} for the memory device with the molecules.

interval of about 1.5 V. A similar discrete shift in the threshold voltage was reported on the silicon nanocrystal based memory device at low temperatures and explained by the single-electron effect [2, 7]. The required voltage increase of ΔV_{GP} for one

electron charging into the dot is calculated by the following equation:

$$\Delta V_{GP} = (\text{quantum energy level spacing} + \text{charging energy}) \times (1 + C_{tt}/C_{CG}),$$

where C_{tt} is the dot-to-channel capacitance and C_{CG} the gate-to-dot capacitance. Assuming that the supramolecular aggregate is a 5 nm spherical conductor in a matrix of SiO_2, the energy level splitting due to quantum effects is estimated to be about 100 meV and the charging energy to be about 74 meV. Then, ΔV_{GP} is calculated to be about 1.4 V, which is close to the measured value of 1.5 V. However, the silicon-based memory devices showed a positive slope in the plot of V_T–V_{GP} due to tunnelling of the electrons from the channel into the nanocrystals, unlike the molecule-based memory device shown in figure 3(c). The appearance of single-electron effects at room temperature is attributed to the uniform size distribution of supramolecular aggregates.

The second notable feature is the staircase plateaus of I_{SD} in nearly equidistant steps with a periodicity ΔV_G of about 2 V. Since the range of the voltage sweep is larger than the required voltage increase of $\Delta V_{GP} \approx 1.5$ V for single-electron charging, the threshold voltage is expected to change during the measurement of the I_{SD}–V_G curve and it causes the staircase behaviour of I_{SD}. We have also measured the retention time of the memory. The retention time is estimated to be about 5 min, which is much shorter than that of the nanocrystal memory device.

4. Summary

We have fabricated hybrid silicon/molecular memory devices using supramolecular rod-bundles that act as quantum dots. The quantized shift in threshold voltage and quantized charging voltage have been observed at room temperature, which are attributed to the single-electron effect. This demonstrates that coupling molecular electronic elements with silicon may enable device structures or devices with improved performance.

Acknowledgments

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